USN | | | | | | | | | | |

06EC56

Fifth Semester B.E. Degree Examination, June/July 2011
Fundamentals of CMOS VLSI

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Describe in detail step-by-step procedure of P-well CMOS fabrication. **(08 Marks)**

b. Explain the transfer plot of CMOS inverter with necessary expression for V_{out} in each region. **(08 Marks)**

c. Write a note on transmission gate. **(04 Marks)**

2 a. Draw circuit diagram and stick diagrams of two input NOR gate using CMOS logic use standard colour/monochrome codes. **(08 Marks)**

b. Explain λ based design rules applicable to MOS layers and transistors. **(08 Marks)**

c. Write a note on Double metal MOS process rules for contact cut. **(04 Marks)**

3 Explain the following logic structures with their salient features:

a. BiCMOS logic b. Pseudo-nMOS logic c. Pass transistor logic d. C^2MOS logic. **(20 Marks)**

4 a. Define sheet resistance, standard unit of capacitance and delay unit of time. **(06 Marks)**

b. Explain cascaded inverters to drive large capacitive loads. Obtain an equation to find number of stages. **(08 Marks)**

c. Discuss the following in scaling of MOS circuits:

i) Limit of miniaturization ii) Limits of interconnect and contact resistance. **(06 Marks)**

PART – B

5 a. Explain the structured design of a parity generator with necessary blocks and stick diagram. **(10 Marks)**

b. Explain domino CMOS logic with neat circuit. **(10 Marks)**

6 a. List and explain the general considerations to be considered in Digital system design. **(06 Marks)**

b. Explain the design of datapath in 4-bit arithmetic processor with floor plan for 4-bit datapath. **(10 Marks)**

c. Write MOS switch implementation of 4×4 crossbar switch. **(04 Marks)**

7 a. What are timing considerations in system design? **(06 Marks)**

b. Draw one-transistor dynamic memory cell circuit arrangement. What is the significance of creating capacitor by using a polysilicon plate over the diffusion area? **(08 Marks)**

c. Explain six transistor static CMOS memory cell arrangement. **(06 Marks)**

8 a. Discuss the requirements of I/O pads in a chip. **(05 Marks)**

b. Explain the sensitized path based testing applied to combinational logic as an example. **(10 Marks)**

c. Write a note on scan design technique. **(05 Marks)**

* * * * *